range from a surface of said source layer to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-40 are presently active. Claims 1, 2, 5-12, and 15-20 have been amended; and Claims 21-40 have been added by the present supplemental amendment. The changes and additions to the claims are supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, Claims 1-3 and 11 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,973,338 to Okabe (hereinafter "the '338 patent"); Claim 4 was rejected under 35 U.S.C. §103(a) as being unpatentable over the '338 patent, further in view of U.S. Patent No. 6,300,663 to Kapor (hereinafter "the '663 patent"); Claim 5 was rejected under 35 U.S.C. §103(a) as being unpatentable over the '338 patent; and Claims 6-10 were rejected under 35 U.S.C. §103(a) as being unpatentable over the '338 and '663 patents, further in view of U.S. Patent No. 6,331,466 to Takahashi et al (hereinafter "the '466 patent").

Amended Claim 1 is directed to a power semiconductor device comprising (1) a base layer of a first conductivity type; (2) a base layer of a second conductivity type; (3) an emitter layer formed on the surface of the base layer of the second conductivity type; (4) a collector layer formed on a surface of the base layer of the first conductivity type; (5) a first main electrode formed on the collector layer; (6) a second main electrode formed on the emitter layer and on the base layer of the second conductivity type; and (7) a gate electrode

formed with first and second insulating films on the base layer of the second conductivity type that lies between the emitter layer and the base layer of the first conductivity type. Claim 1 has been amended to recite an emitter layer (instead of one of an emitter layer and a source layer), and a collector layer (instead of one of an collector layer and a drain layer). Dependent Claims 2 and 5-10 have been amended accordingly.

Amended Claim 11, directed to a method of manufacturing a power semiconductor device, recites limitations analogous to the limitations recited in Claim 1. Note that Claim 11 (and dependent Claims 12 and 15-20) have also been amended by the present amendment to specifically recite an emitter layer and a collector layer.

Applicants respectfully submit that Claims 1-20 are patentable over the '338, '663, and '466 patents for the reasons set forth in the amendment filed May 20, 2002, and that the patentability of Claims 1-20 with respect to the cited references is not altered based on the present amendment.

The present amendment also sets forth new Claims 21-40 for examination on the merits. Claims 21-40 recite limitations analogous to the limitations recited in Claims 1-20, respectively, except that Claims 21-40 recite a source layer and a drain layer. Thus, new Claims 21-40 are supported by the originally filed specification and do not add new matter. Moreover, Applicants submit that Claims 21-40 are patentable based on the patentability of Claims 1-20.

Thus, it is respectfully submitted that independent Claim 1 (and dependent Claims 2-10), independent Claim 11 (and dependent Claims 12-20), independent Claim 21 (and dependent Claims 22-30), and independent Claim 31 (and dependent Claims 32-40) patentably define over the cited references.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds of rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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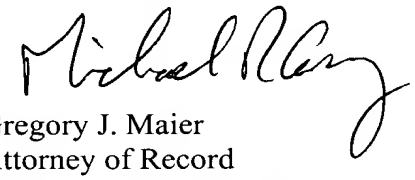

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Please amend Claims 1, 2, 5-12, and 15-20 as follows.

1. (Twice Amended) A power semiconductor device comprising:

a base layer of a first conductivity type;

a base layer of a second conductivity type selectively formed on one surface of said base layer of the first conductivity type;

[one of] an emitter layer [and a source layer] of the first conductivity type selectively formed on the surface of said base layer of the second conductivity type;

[one of] a collector layer [and a drain layer] selectively formed on one of the one surface and another surface of said base layer of the first conductivity type;

a first main electrode formed on said [one of said] collector layer [and said drain layer];

a second main electrode formed on said [one of said] emitter layer [and said source layer] and on said base layer of the second conductivity type; and

a gate electrode formed with first and second gate insulating films on said base layer of the second conductivity type that lies between [said one of] said emitter layer [and said source layer] and said base layer of the first conductivity type,

wherein a capacitance of a capacitor formed on the second gate insulating film is different from a capacitance of a capacitor formed on the first gate insulating film.

2. (Twice Amended) The power semiconductor device according to claim 1, wherein the first gate insulating film is formed in a portion near said [one of said] emitter layer [and said source layer], and the second gate insulating film is formed in a portion near said base layer of the first conductivity type.

5. (Twice Amended) The power semiconductor device according to claim 2, wherein a thickness of the second gate insulating film has an inclination and the thickness thereof on a side of said [one of said] emitter layer [and said source layer] is smaller than a thickness on a side of said base layer of the first conductivity type.

6. (Twice Amended) The power semiconductor device according to claim 1, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of [said one of] said emitter layer [and said source layer] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

7. (Twice Amended) The power semiconductor device according to claim 2, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of [said one of] said emitter layer [and said source layer] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

8. (Twice Amended) The power semiconductor device according to claim 3, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of [said one of] said emitter layer [and said source layer] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

9. (Twice Amended) The power semiconductor device according to claim 4, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of [said one of] said emitter layer [and said source layer] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

10. (Twice Amended) The power semiconductor device according to claim 5, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of [said one of] said emitter layer [and said source layer] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

11. (Twice Amended) A method of manufacturing a power semiconductor device comprising:

forming a base layer of a first conductivity type;

selectively forming a base layer of a second conductivity type on one surface of the base layer of the first conductivity type;

selectively forming [one of] an emitter layer [and a source layer] of the first conductivity type on a surface of the base layer of the second conductivity type;

selectively forming [one of] a collector layer [and a drain layer] on one of the one surface and another surface of the base layer of the first conductivity type;

forming a first main electrode on said [one of the] collector layer [and the drain layer];

forming a second main electrode on said [one of the] emitter layer [and the source layer of the first conductivity type] and on the base layer of the second conductivity type; and

forming first and second gate insulating films on the base layer of the second conductivity type that lies between said [one of the] emitter layer [and the source layer of the first conductivity type] and the base layer of the first conductivity type and forming a gate electrode on the first and second gate insulating films;

wherein a capacitance of a capacitor formed on the second gate insulating film is different from a capacitance of a capacitor formed on the first gate insulating film.

12. (Amended) The method of manufacturing a power semiconductor device according to claim 11, wherein the first gate insulating film is formed in a portion near [said one of] said emitter layer [and source layer] and the second gate insulating film is formed in a portion near said base layer of the first conductivity type.

15. (Amended) The method of manufacturing a power semiconductor device according to claim 12, wherein a thickness of the second gate insulating film has an

inclination and the thickness thereof on a side of [said one of] said emitter layer [and said source layer] is smaller than a thickness on a side of said base layer of the first conductivity type.

16. (Amended) The method of manufacturing a power semiconductor device according to claim 11, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of [said one of] said emitter layer [and said source layer] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

17. (Amended) The method of manufacturing a power semiconductor device according to claim 12, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of [said one of] said emitter layer [and said source layer] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

18. (Amended) The method of manufacturing a power semiconductor device according to claim 13, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of [said one of] said emitter layer [and said source layer] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

19. (Amended) The method of manufacturing a power semiconductor device according to claim 14, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of [said one of] said emitter layer [and said source layer] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

20. (Amended) The method of manufacturing a power semiconductor device according to claim 15, wherein said gate electrode is buried in a trench with the first and second gate insulating films disposed therebetween to form a trench structure, the trench being formed to range from a surface of [said one of] said emitter layer [and said source layer] to an intermediate portion of said base layer of the first conductivity type via said base layer of the second conductivity type.

21-40. (New)